Millimeter-Wave GaAs Monolithic Multipliers

John Papapolymerou, Jack East and Linda P.B. Katehi
EECS Department, The University of Michigan, Ann Arbor, Michigan

Moonil Kim and Imran Mehdi
Jet Propulsion Laboratory, Pasadena, California

Abstract

This paper describes the design, fabrication and experimental results for planar monolithic multipliers with output frequencies in W and D band. The multipliers are fabricated using FGC (Finite Ground Coplanar) lines which provide a low loss, low dispersion near TEM structure. This structure allows circuit fabrication on full thickness wafers with no via holes. A variety of circuits have been designed and fabricated. Different W band multipliers have an output efficiency of 22.9%, a peak output power of 66 milliwatts and an output bandwidth greater than 8 GHz in W band. Initial D band results show an uncalibrated output of approximately $100\mu W$ at 160 GHz.

I Introduction

Local oscillators are an important part of all high frequency receivers. Most high frequency multipliers use waveguide mounts. The advantages of waveguide multipliers include high Q low loss circuits, ease of tuning with E-H tuners available on both the input and output ports and a natural high pass filter configuration with cutoff waveguides. However, waveguide mount structures become smaller and more difficult to fabricate with increasing frequency. Planar monolithic multipliers provide an alternative fabrication approach that results in smaller size and volume. At the same time, they can be batch fabricated using integrated circuit techniques with lower cost than waveguide circuits. On the other hand monolithic multipliers have limitations such as higher loss and lower Q than waveguide circuits, while they lack the capability for post fabrication tuning. Conventional circuit components fabricated with microstrip lines or CPW have to be carefully designed to avoid moding at higher frequencies. A summary of some of the design tradeoffs for waveguide and monolithic multipliers along with a survey of experimental performance is given in [1]-[2].

The FGC (Finite Ground Coplanar) line is an alternative guiding structure that overcomes many of the limitations of the microstrip or CPW when operating at high frequencies. This line is similar in cross section to CPW, except that the grounds are narrow and thus prevent the parallel plate mode that can limit the high frequency operation. The resulting line supports a nearly ideal TEM propagation and can operate without backside metallization. The measured effective dielectric constant of the line is nearly constant from low frequencies up to 118 GHz and the attenuation in db/λ_g is $\propto 1/\sqrt{f}$, indicating that ohmic loss is the dominant effect. Due to the frequency dependence of ohmic losses, multipliers with FGC lines scaled at higher frequencies will experience less loss. Measured results along with more details on FGC lines that can be found in [3], show an attenuation of 0.22 dB/λ_g at 100 GHz.

II Multiplier Design

Waveguide multipliers are typically designed around an existing varactor diode. The diode capacitance vs. bias voltage and an estimate of the diode series resistance vs. bias and frequency are the electrical input parameters. The mounting structure must

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

be designed around the varactor contact geometry. In contrast, in a monolithic multiplier the diode and the circuit are designed together. The first step is to choose the epitaxial layer doping that depends on the frequency and the expected electric fields which lead to possible velocity saturation in the undepleted portion of the epitaxial layer during the RF cycle. A description of velocity saturation effects is given in [4]. The design tradeoff is between a low doping to increase the breakdown voltage and the amount of power that can be absorbed before breakdown, and a higher doping to reduce the saturation effects. The wafers used in this study have an epitaxial layer doping of $10^{17}/cm^3$ and an epitaxial layer thickness of $4000\mathring{A}$. This doping level has been optimized for the W band multipliers but it was low for the D band circuits.

A nonlinear multiple reflection computer program based on [5] was written to optimize the multiplier design. The input design parameters are the epitaxial layer doping and thickness, GaAs material parameters, the desired real diode impedance and the Q at the pump frequency. The output data from this program are the embedding impedance at the second harmonic frequency, the required diode area and the estimated reverse bias voltage. The program calculates this output information for a range of input pump power levels and chooses a set of design parameters. The W band multipliers in this study have been designed with input quality factors of 2 and 3 and diode areas of 74 and 65 μm^2, respectively. The D band multipliers have a design Q of 2, and single diode areas of 40, 45 and 50 μm^2.

The next step is circuit realization using FGC lines. The dimensions of the FGC lines are limited by lithography and as a result the range of line impedances is approximately 20 to 100 Ω. Stubs are used on the input side of the circuit to trap the second harmonic output and on the output side to trap the local oscillator frequency. The diode capacitance is tuned with an inductive line connected to the circuit. The W and D band circuits, along with calibration lines and process monitors become part of the same mask set. This mask set has been used to fabricate the experimental circuits, a sample of which can be seen in Fig. 1.

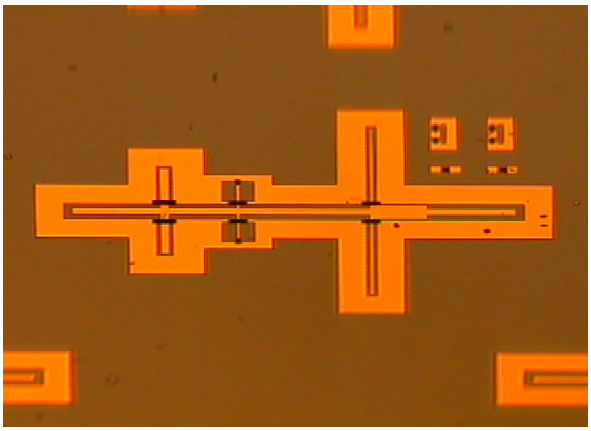

Figure 1: FGC line W-Band multiplier.

III Results and Discussion

In this section measured results from the W and D band multipliers that have been fabricated are presented.

III.1 *W-Band Multipliers*

The W band circuits have a Ka band input measurement system with a planar probe at the input and a W band probe with a waveguide section at the output. The measurements are vector error corrected to the tips of the measurement probes using a two tier error correction. A one port waveguide (Short, Offset Short, Load) calibration is used to calibrate to a waveguide flange where power can be measured with a waveguide power meter. A second one port SOL (Short Open Load) calibration is used to evaluate the waveguide to coaxial transition, a cable and the probe that form the rest of the input measurement system. The two sets of correction coefficients are combined to obtain the input port available power and return loss. A SOL one port calibration is used to find the correction coefficients between the W band probe tip at the multiplier output and the waveguide flange location of the output power meter.

Two W band multipliers with designed Q's of 2 and 3 are evaluated. Based on simulation predictions, the low Q circuits are expected to have wider bandwidths and lower efficiencies than the higher Q versions. The high Q designs have higher peak electric fields, peak depletion layer voltages and DC reverse bias. The peak voltages in the Q=3 structures are closer to the experimental reverse breakdown voltage than the ones for Q=2. These predictions have been confirmed by the measurements. Results for the input Q = 2 circuit are shown in Figs. 2 and 3. Fig. 2 shows the output power and efficiency vs. input power for an input frequency of 38.15 GHz. The output power is limited by the available power of the measurement system. A peak power of 66 mW has been measured at 76.3 GHz. Fig. 3 shows the multiplier efficiency and return loss for a constant input drive of 20 dBm. The measurement accuracy is limited on the 80 GHz high end by the upper limit of the input Ka band system and the observed ripple is due to a standing wave in the coaxial cable between the input waveguide measurement system and the input coaxial probe. The peak efficiency is 17.2% at 76.3 GHz with a return loss of -4 dB and the -3 dB bandwidth is approximately 7.5 GHz. Results for the input Q = 3 circuit are shown in Fig. 4, where a bandwidth of approximately 6 GHz can be observed. The multiplier peak efficiency of 22.9% with a retun loss of -5 dB occurs at an input power level of 17 dBm, a much lower level than the Q = 2 circuit. The combination of a 6 GHz bandwidth with an efficiency of 22.9% makes this multiplier design unique since it offers both a very good efficiency and a broad bandwidth.

III.2 *D-Band Multipliers*

The D band circuits have a W band input probe and a D band output probe. The D band probe is a prototype and as a result the output power measurement is not calibrated since only the range of its insertion loss is known (3-6 dB). Figures 5 and 6 show the measured results for the D-Band multipliers. The input power for the frequency range of 78 to 90 GHz varies between 7.3 and 14 mW. An uncalibrated conversion loss of 20.72 dB (0.85% efficiency) is achieved at 160 GHz with the diode unbiased, and with a bias of -0.7 V an output power of $100\mu W$ is detected. Based on the minimum value of the output probe loss the output power is estimated to be $200\mu W$, while the multiplier bandwidth is measured to be 5 GHz. Other waveguide based multipliers in this frequency range have higher efficiency but are narrow band. Improvement of the D band multiplier efficiency can be achieved by appropriately optimizing the epitaxial layer profile.

The results presented herein show that scaling the FGC multiplier design to higher frequencies can still provide a reasonable efficiency while maintaining the excellent bandwidth.

IV Acknowledgments

This work was supported by the Office of Naval Research and Texas Instruments. The authors would also like to acknowledge Todd Gaier and Peter Siegel's help with the D band measurements at JPL.

References

[1] "Finite Ground Coplanar Passive and Active Circuits," Fred Brauchler, Ph.D thesis, The University of Michigan, Ann Arbor, Michigan, 1996.

[2] Fred Brauchler, John Papapolymerou, Jack East and Linda Katehi, "W Band Monolithic Multipliers," 1997 IEEE MTT-S Symposium Digest pp 1225-1228.

[3] Fred Brauchler, Steve Robertson, Jack East and Linda Katehi, "W Band Finite Ground Coplanar (FGC) Line Circuit Elements," 1996 IEEE MTT-S Symposium Digest , pp 1845-1848.

[4] J. East. E. Kollberg and M. Frerking, "Performance limitations of Varactor Multipliers," Proceedings of the Fourth International Symposium on Space Terahertz Technology, pp 312-325, March, 1993.

[5] "Microwave Mixers," S. Mass, Artech House, 1986.

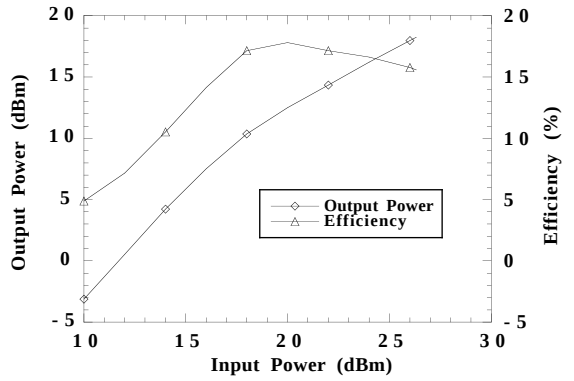

Figure 2: Efficiency and output power vs. input power at f=38.15 GHz for a Q=2 multiplier.

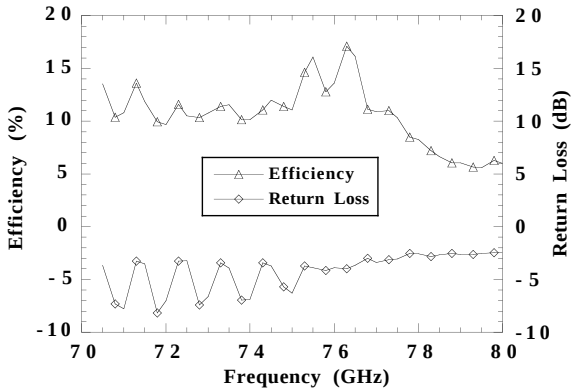

Figure 3: Efficiency and return loss vs. output frequency at P_{in}=20 dBm for a Q=2 multiplier.

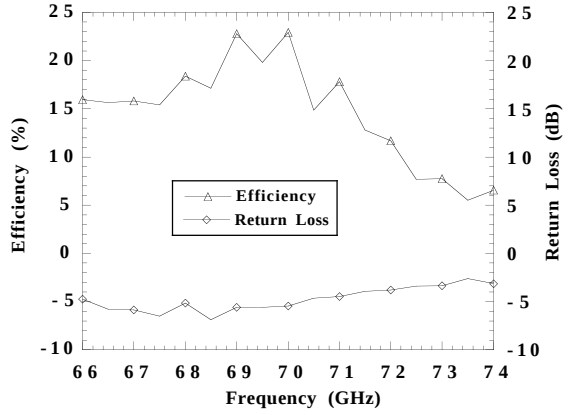

Figure 4: Efficiency and return loss vs. output frequency at P_{in}=17 dBm for a Q=3 multiplier.

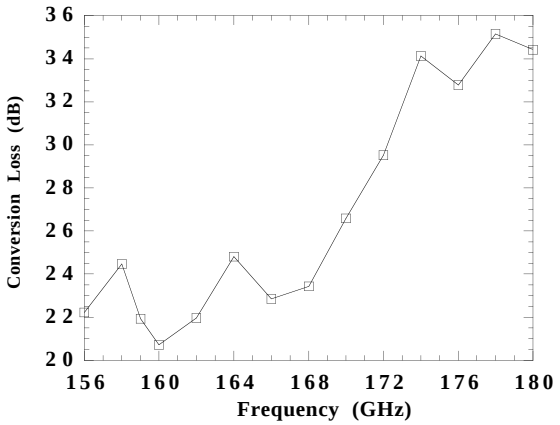

Figure 5: Conversion loss vs. output frequency for a Q=2 multiplier at zero diode bias. The results are not calibrated.

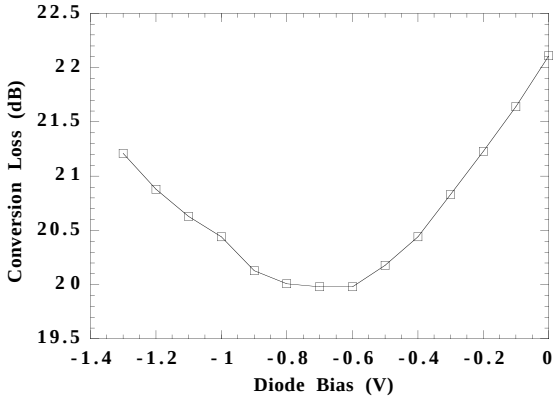

Figure 6: Conversion loss vs. diode bias at P_{in}=10 dBm and f=160 GHz for a Q=2 multiplier. The results are not calibrated.